

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:
 - a plurality of word lines;
 - a plurality of bit lines; and
 - a memory circuit including a plurality of memory cells each connected to one of said plurality of word lines and one of said plurality of bit lines,
 - wherein said memory circuits performs:
 - an operation of selecting every other word line in said plurality of word lines in a first test mode;
 - an operation of setting all of the plurality of word lines to a selected state and applying a ground potential of the circuit to all of said plurality of bit lines in a second test mode;
 - an operation of applying a predetermined potential to every other bit line in the plurality of bit lines and applying a ground potential of the circuit to the other bit lines in a third test mode; and
 - an operation of setting all of the plurality of bit lines at a predetermined potential corresponding to a selection level of the bit lines and setting all of said plurality of word lines to a non-selection state in a fourth test mode.
 2. The semiconductor device according to claim 2, further comprising:
 - a microprocessor for accessing said memory circuit

and a mode control circuit,

wherein a test mode is set to said mode control circuit, thereby setting the microprocessor into a standby mode and setting said memory circuit in any of said first to fourth test modes.

3. The semiconductor device according to claim 3, wherein said memory circuit is a mask ROM.

4. A method of testing a semiconductor device comprising a plurality of word lines, a plurality of bit lines, and a memory circuit including a plurality of memory cells each connected to one of said plurality of word lines and one of said plurality of bit lines, the method comprising:

selecting every other word line in said plurality of word lines in a first test mode;

setting all of the plurality of word lines to a selected state and applying a ground potential of the circuit to all of said plurality of bit lines in a second test mode;

applying a predetermined potential to every other bit line in the plurality of bit lines and applying a ground potential of the circuit to the other bit lines in a third test mode;

setting all of the plurality of bit lines at a predetermined potential corresponding to a selection

level of the bit lines and setting all of said plurality of word lines to a non-selection state in a fourth test mode;

measuring current passed to a power supply terminal of the semiconductor device in said first to fourth test modes and detecting a short circuit between word lines, a short circuit between bit lines, and a short circuit between a word line and a bit line.

5. The method of testing a semiconductor device according to claim 4,

wherein said semiconductor device further comprises a microprocessor for accessing the memory circuit and a mode control circuit, and

wherein the method further comprises:

setting the microprocessor into a standby mode and setting said memory circuit in any of said first to fourth test modes by setting a test mode to said mode setting circuit so that said current passed to said power supply terminal in accordance with each of the first to fourth test modes is measured.

6. The method of testing a semiconductor device according to claim 5, further comprising:

conducting a direct current test on the semiconductor device at the time of a probe test of said semiconductor device; and

conducting a direct current test on the semiconductor device,

wherein said detection of a short circuit in any of said first to fourth test modes is performed on said memory circuit.

7. The method of testing a semiconductor device according to claim 6,

wherein said detection of a short circuit of said memory circuit is conducted on said semiconductor device which is determined as a non-defective in the direct current test on said semiconductor device, and

wherein said alternate current test is conducted on said memory circuit having no short circuit.

8. The method of testing a semiconductor device according to claim 7,

wherein the semiconductor device subjected to said probe test is assembled and subjected to aging, thereafter, said direct current test is conducted on the semiconductor device,

wherein said detection of a short circuit is performed in said first to fourth test modes on said memory circuit, and

wherein said alternating current test is conducted on the semiconductor device.

9. The method of testing a semiconductor device according to claim 8,

wherein said detection of a short circuit in said memory circuit is made on said semiconductor device which has been determined as a non-defective in the direct current test, and

wherein said alternating current test is conducted on said semiconductor device having no short circuit in said memory circuit.